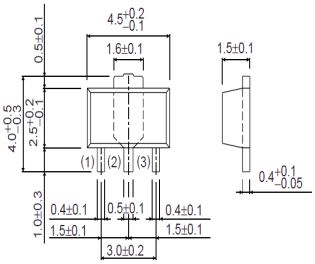
Leiditech

LMXD6072

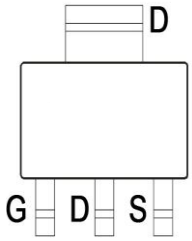
N-Channel Enhancement Mode Field Effect Transistor

Main Product Characteristics:

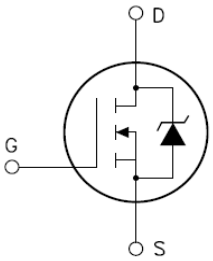
V_{DSS}	60V
R_{DS}(on)	67mΩ (typ.)
I_D	4A



SOT-89-3L



Marking and pin Assignment



Schematic diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for DC-DC and DC-AC converters, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature
- Automotive

Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in DC-DC and DC-AC converters and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	4	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	3	
I_{DM}	Pulsed Drain Current②	16	
P_D @TC = 25°C	Power Dissipation③	3.3	W
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	15	mJ
I_{AS}	Avalanche Current @ L=0.3mH	10	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	38	℃/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	35	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

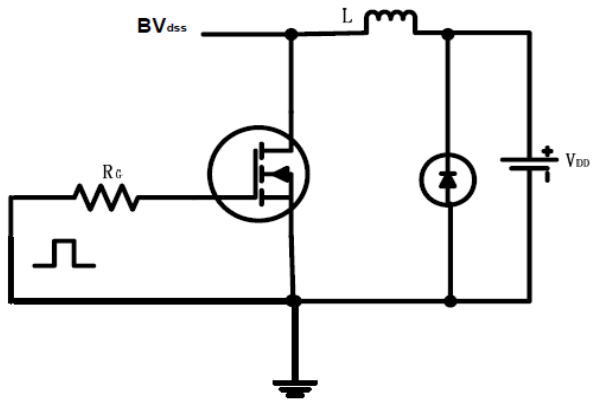
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	67	100	mΩ	V_{GS}=10V,I_D = 1.5A
		—	76	115		V_{GS}=5V,I_D = 1.5A
$V_{GS(th)}$	Gate threshold voltage	1	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 60V,V_{GS} = 0V
		—	—	10		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =20V
		—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	1	—	—	S	V_{DS} = 15 V I_D = 1.5A
Q_g	Total gate charge	—	12	—	nC	I_D = 4A,
Q_{gs}	Gate-to-Source charge	—	3.5	—		V_{DS}=40V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	3.7	—		V_{GS} =10V
$t_{d(on)}$	Turn-on delay time	—	9.2	—	ns	V_{GS}=10V, VDS=25V, R_{GEN}=50Ω， I_D = 1.2A,
t_r	Rise time	—	16.7	—		
$t_{d(off)}$	Turn-Off delay time	—	35.4	—		
t_f	Fall time	—	8.6	—		
C_{iss}	Input capacitance	—	582	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	49	—		V_{DS} = 30V
C_{rss}	Reverse transfer capacitance	—	36	—		f = 1MHz

Source-Drain Ratings and Characteristics

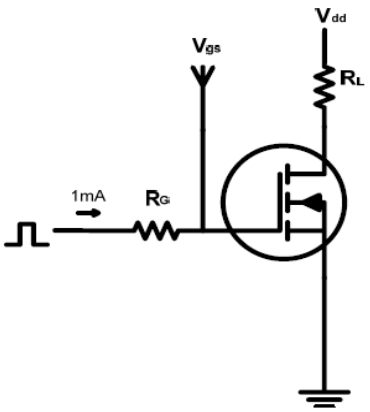
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	16	A	
V_{sd}	Diode Forward Voltage	—	—	1.5	V	I_S=4A, V_{GS}=0V

Test circuits and Waveforms

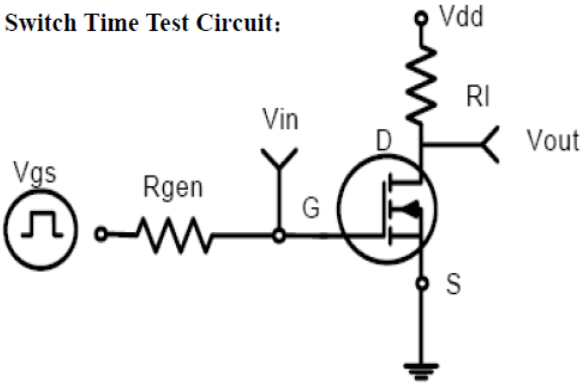
EAS test circuits:



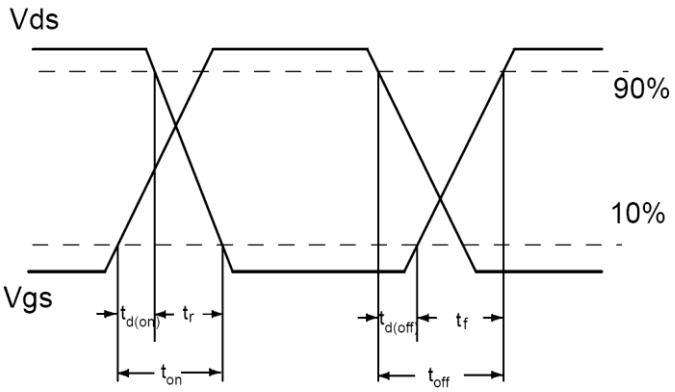
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

①The maximum current rating is limited by bond-wires.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to- ambient thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical electrical and thermal characteristics

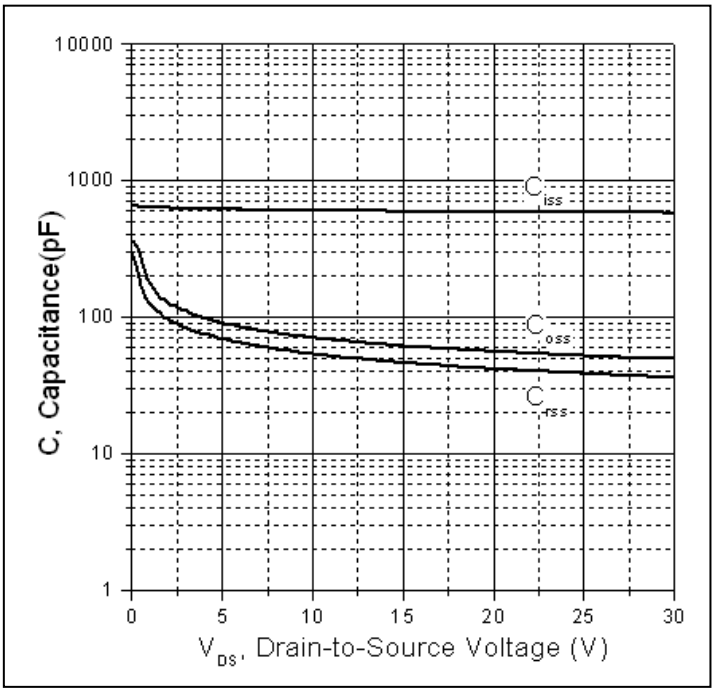


Figure 1: Typical Capacitance Vs. Drain-to-Source Voltage

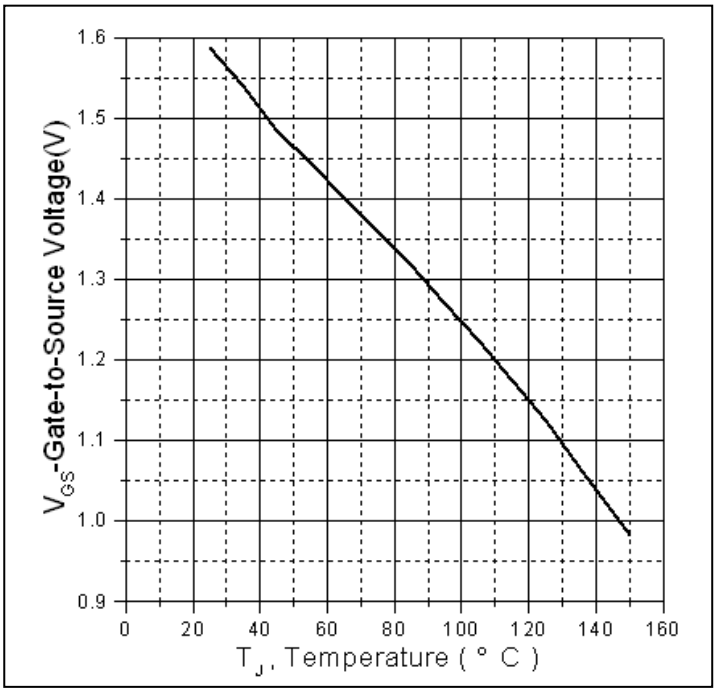


Figure 2. Gate to source cut-off voltage

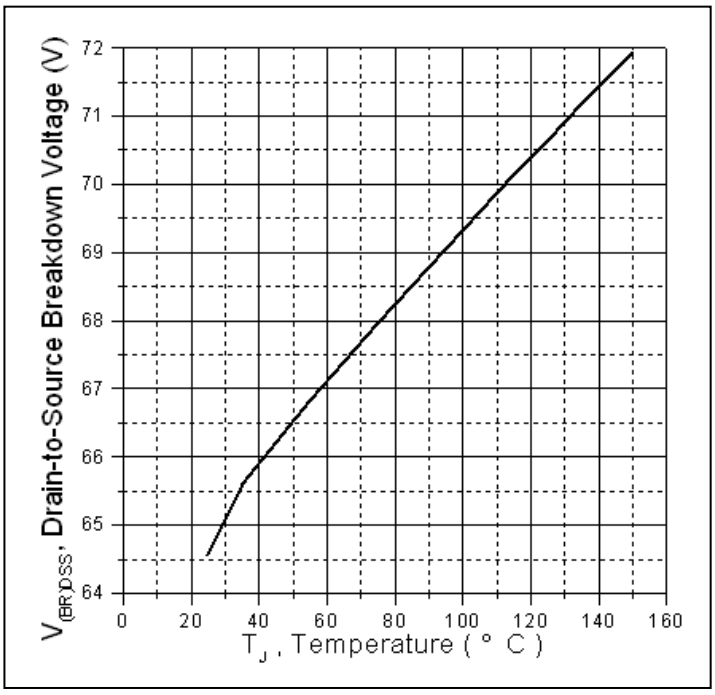


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

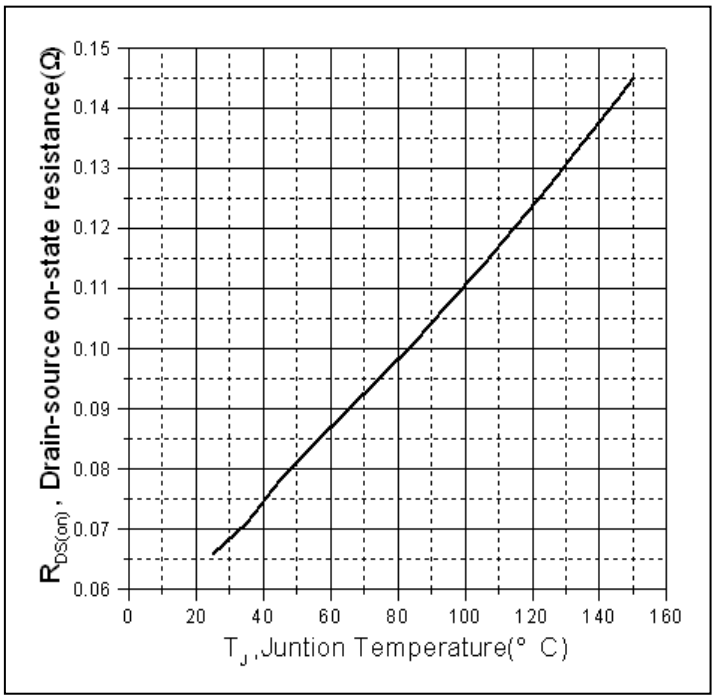


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

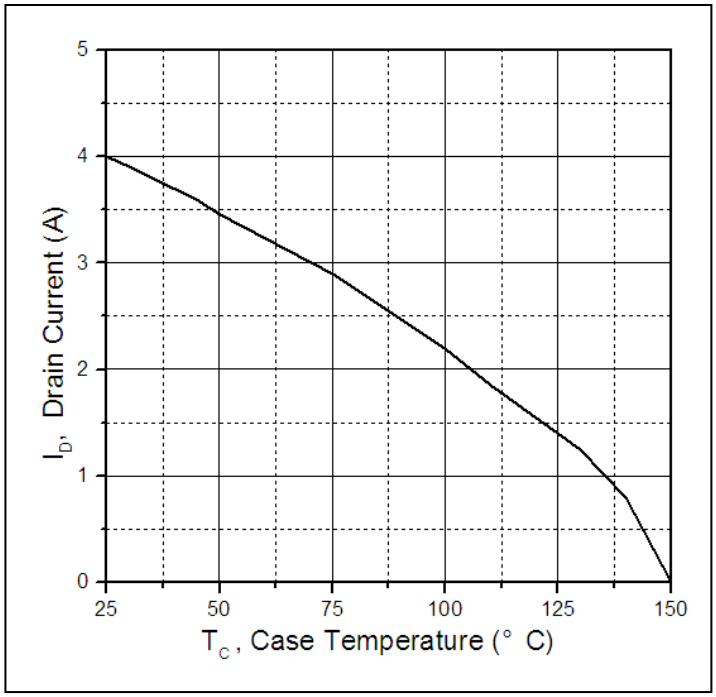


Figure 5. Maximum Drain Current Vs. Case Temperature

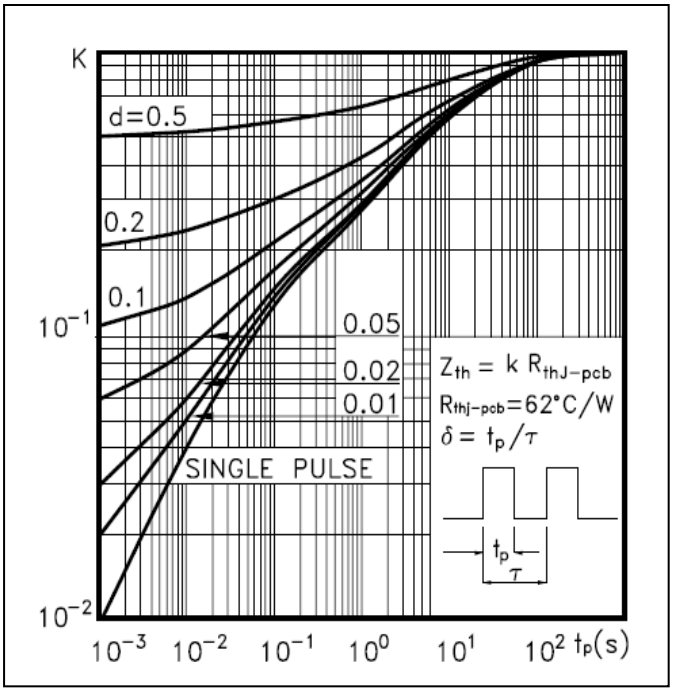
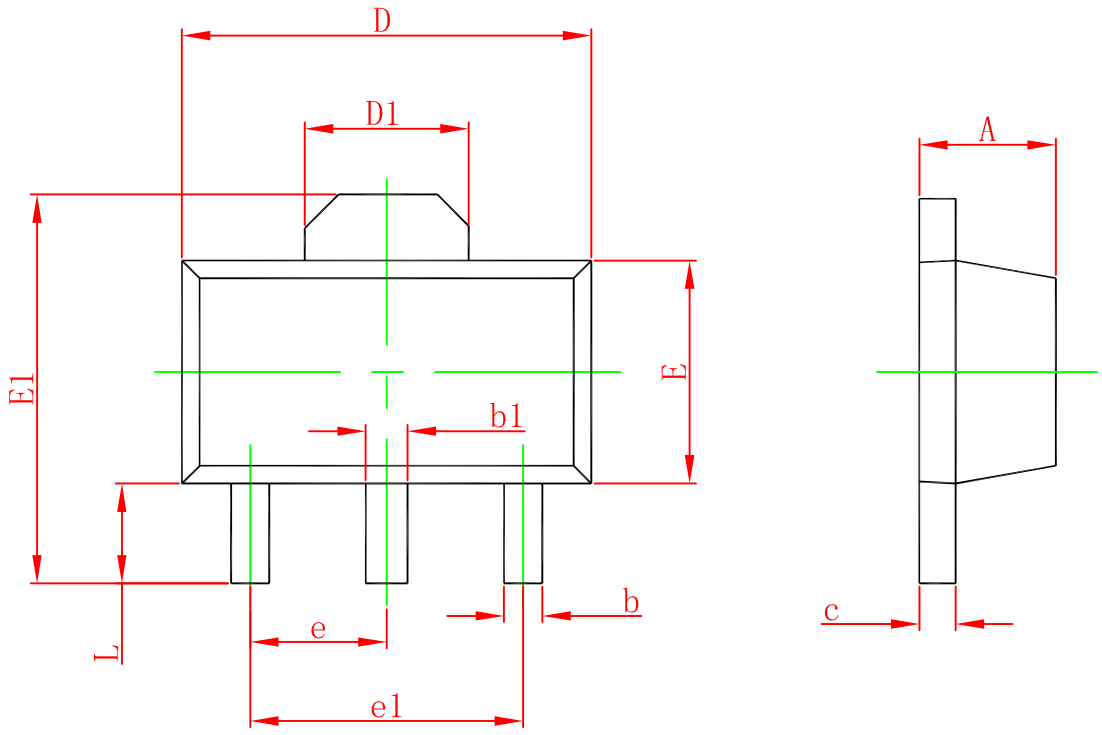


Figure 6. Maximum Effective Transient Thermal Impedance, Junction-to-Case

SOT-89-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

Ordering and Marking Information

Device Marking: **XD6072**

Package (Available)

SOT-89-3L

Operating Temperature Range

C : -55 to 175ºC

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ or 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=125℃ or 150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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