



## LCE P-Channel Enhancement Mode Power MOSFET

**Description**

The LCE60P65K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for high current load applications.

**General Features**

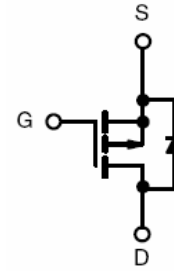
- $V_{DS} = -60V, I_D = -65A$   
 $R_{DS(ON)} < 18m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

**Application**

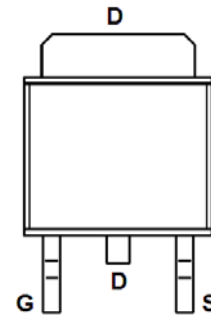
- Load switch

**100% UIS TESTED!**

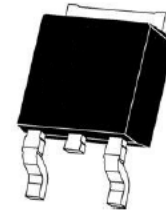
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE60P65K	LCE60P65K	TO-252-2L	-	-	-

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-65	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	-42.3	A
Pulsed Drain Current	$I_{DM}$	-260	A
Maximum Power Dissipation	$P_D$	130	W
Derating factor		0.87	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	722	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.15	$^{\circ}C/W$
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**Electrical Characteristics ( $T_C=25^{\circ}C$  unless otherwise noted)**

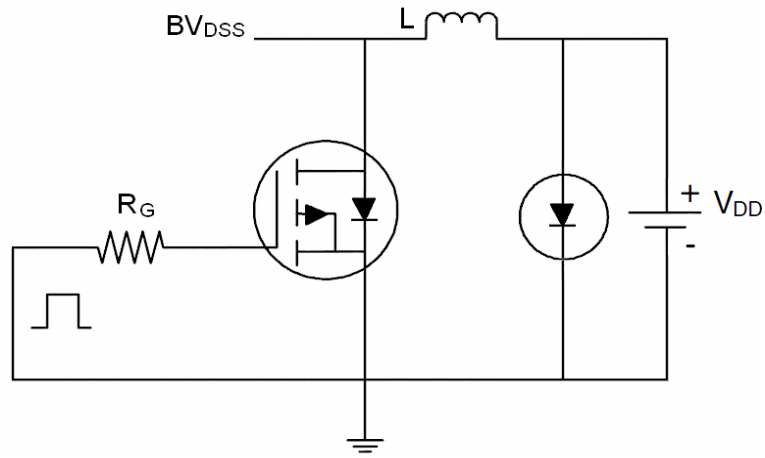
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2.0	-2.6	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	13	18	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-5V, I_D=-20A$	-	25	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0MHz$	-	5814	-	PF
Output Capacitance	$C_{oss}$		-	483	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	234	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	18	-	nS
Turn-on Rise Time	$t_r$		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	$t_f$		-	35	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30, I_D=-20A,$ $V_{GS}=-10V$	-	75	-	nC
Gate-Source Charge	$Q_{gs}$		-	16	-	nC
Gate-Drain Charge	$Q_{gd}$		-	19	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=-20A$	-	-	-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	-65	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = -20A$ $di/dt = -100A/\mu s$ <sup>(Note 3)</sup>	-	49	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	71	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

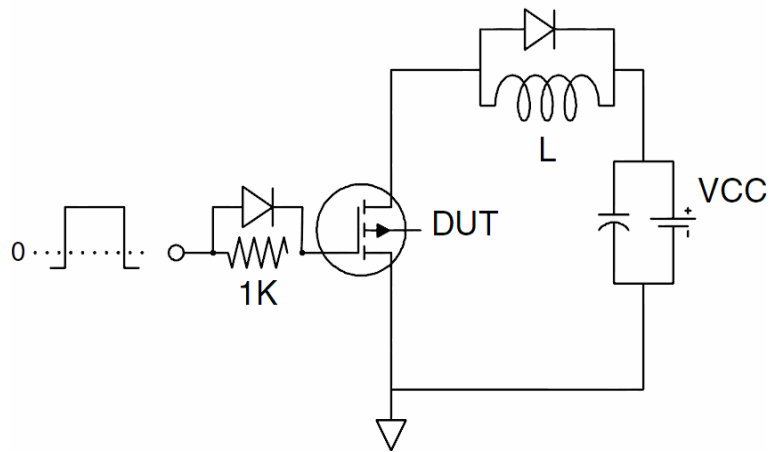
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}C, V_{DD}=-30V, V_G=-10V, L=0.5mH, R_g=25\Omega$

**Test Circuit**

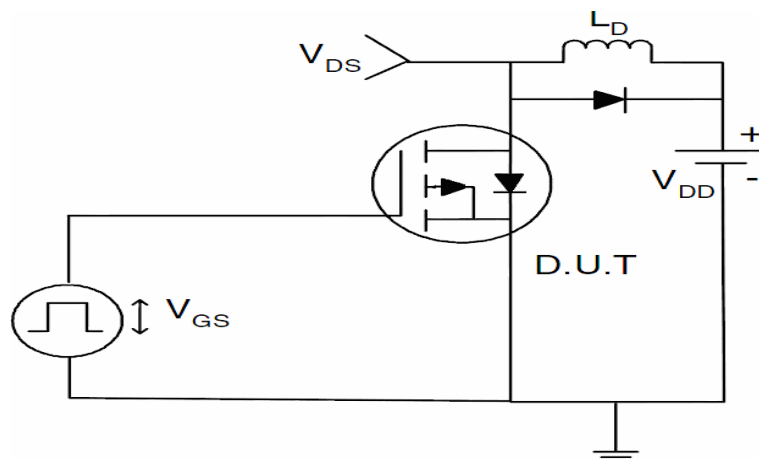
**1) E<sub>AS</sub> Test Circuit**



**2) Gate Charge Test Circuit**



**3) Switch Time Test Circuit**





### Typical Electrical and Thermal Characteristics (Curves)

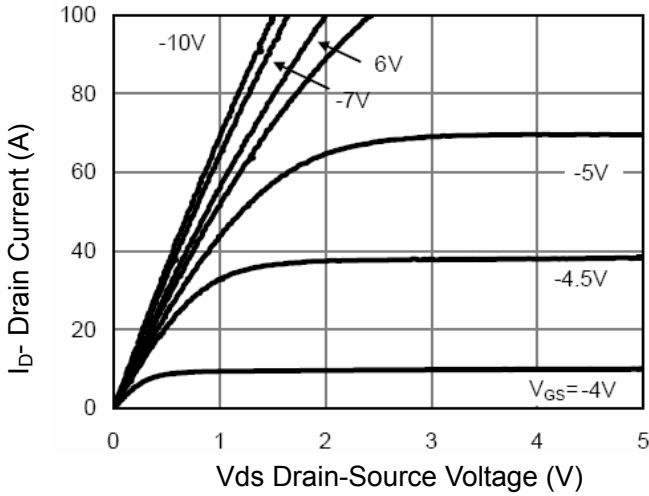


Figure 1 Output Characteristics

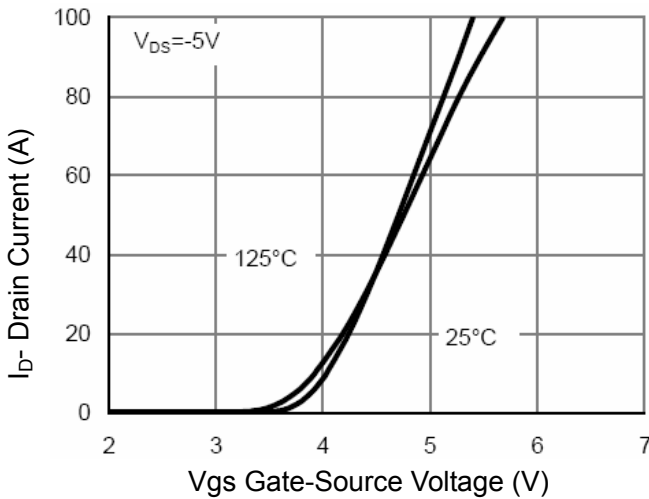


Figure 2 Transfer Characteristics

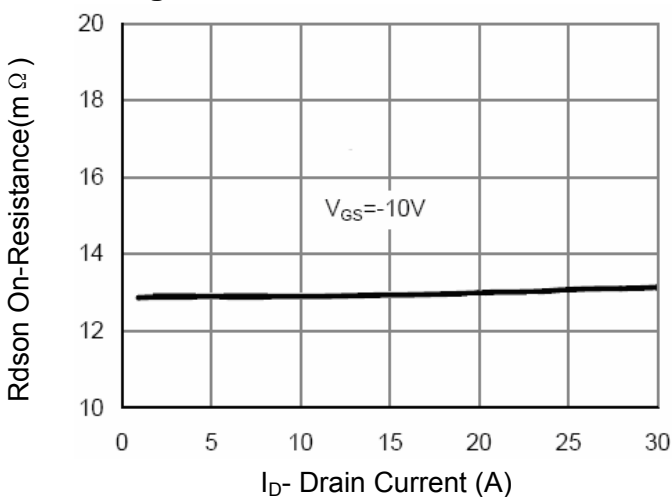


Figure 3  $R_{Dson}$ - Drain Current

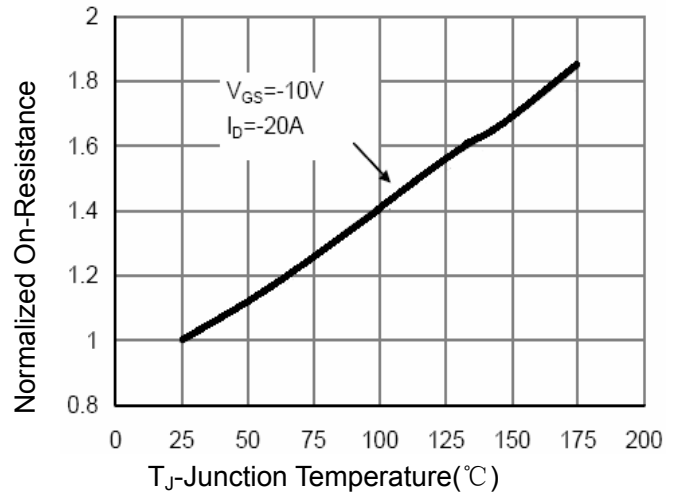


Figure 4  $R_{Dson}$ -Junction Temperature

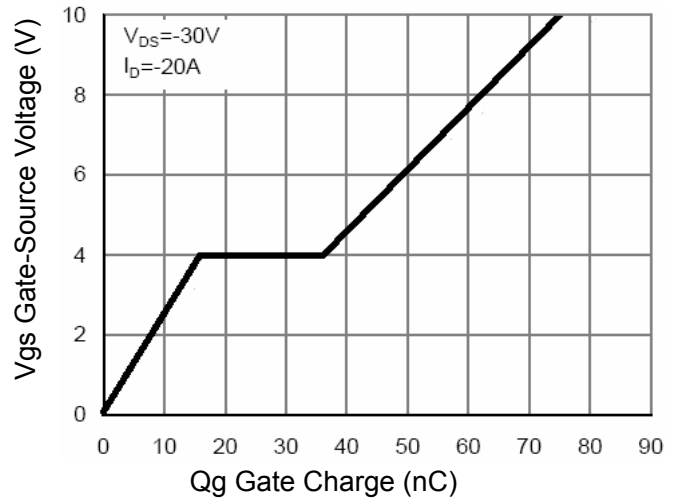


Figure 5 Gate Charge

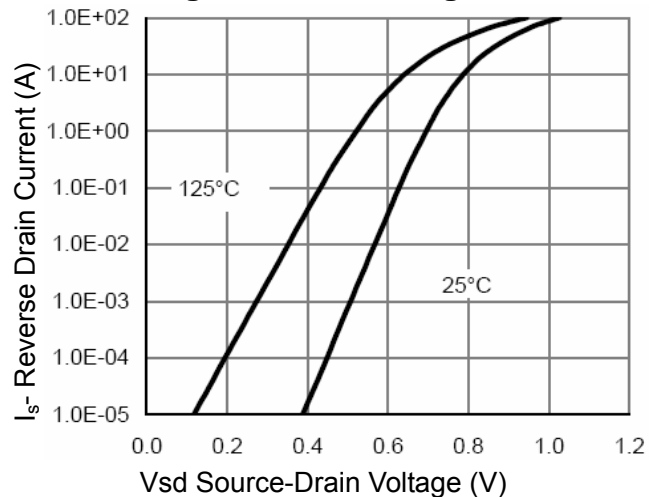


Figure 6 Source- Drain Diode Forward

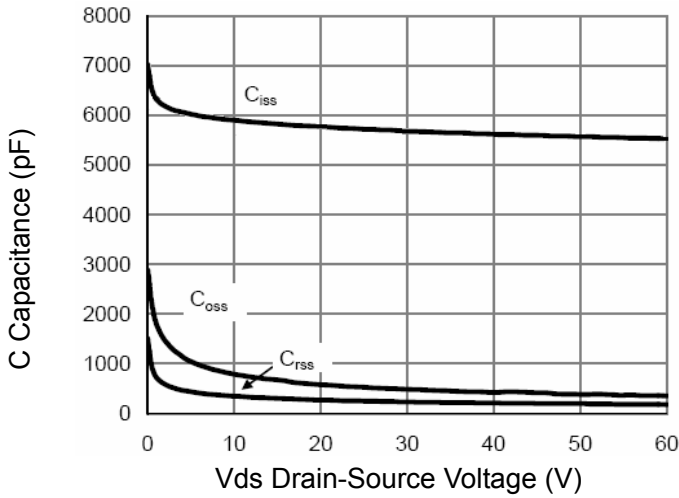


Figure 7 Capacitance vs Vds

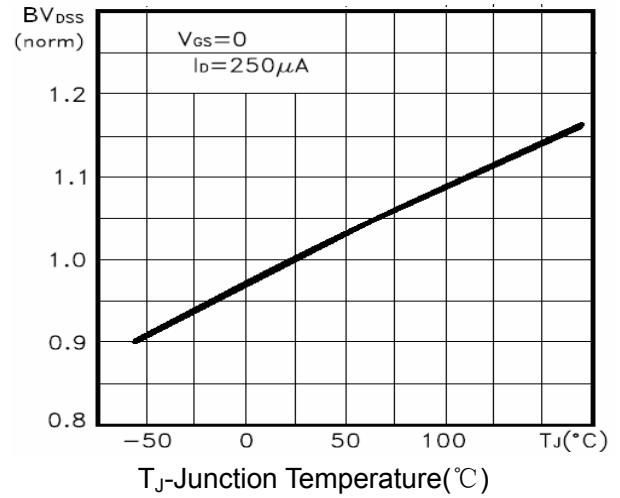


Figure 9  $BV_{DSS}$  vs Junction Temperature

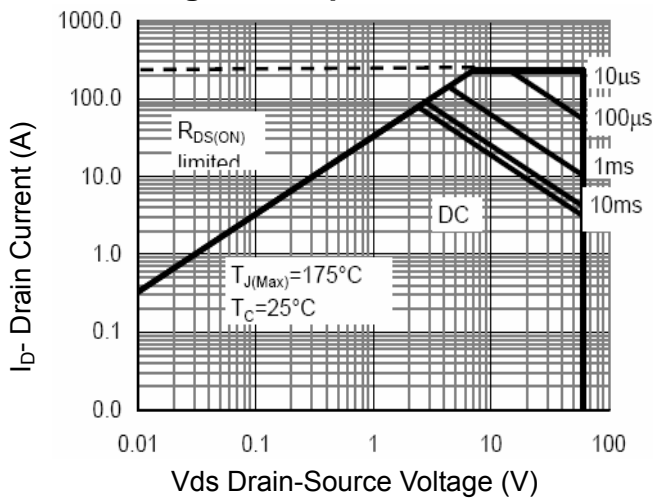


Figure 8 Safe Operation Area

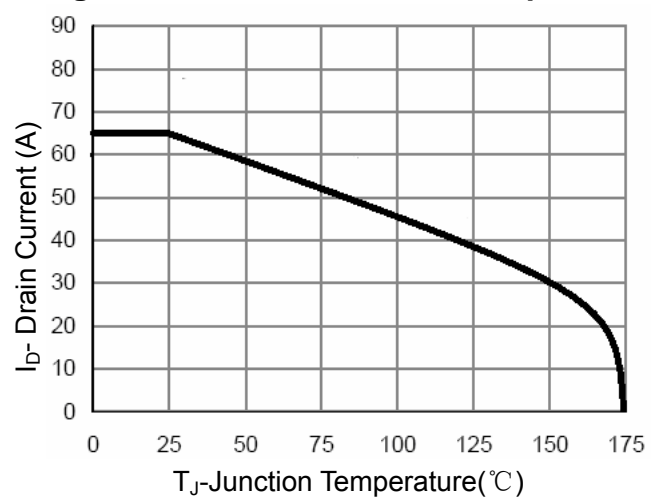


Figure 10  $I_D$  Current Derating vs Junction Temperature

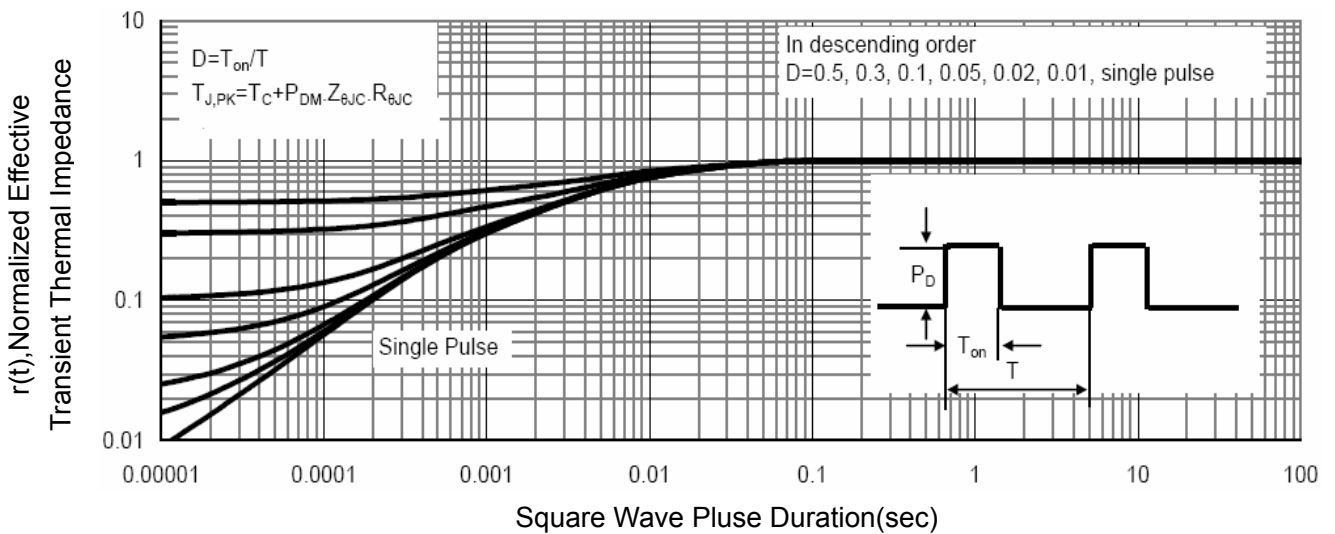
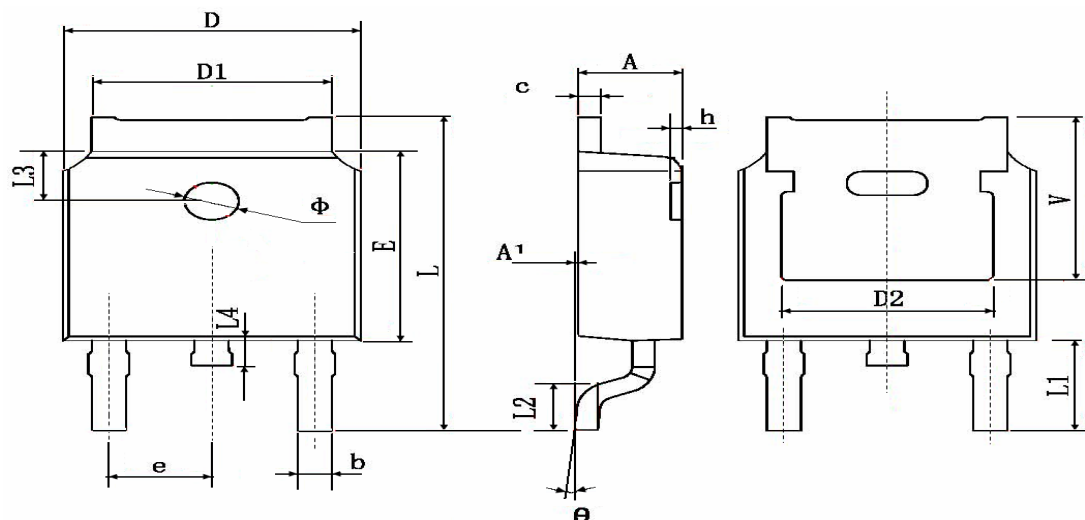


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

Shanghai Leiditech Electronic Co.,Ltd  
 Email: sale1@leiditech.com  
 Tel : +86- 021 50828806  
 Fax : +86- 021 50477059